CLAIMS

We claim:

1. A method for producing a circuit description of a design, the method comprising:

a) from the design, selecting a candidate sub-network that includes multiple circuit elements;

b) generating a parameter based on a set of output functions performed by the selected candidate sub-network;

c) using the parameter to retrieve a replacement sub-network from a storage structure that stores replacement sub-networks;

d) determining whether to replace the selected candidate sub-network with the replacement sub-network in the design;

e) if determine to replace the selected candidate sub-network, replacing the selected candidate sub-network with the replacement sub-network in the design.

2. A method for producing a circuit description of a design, the method comprising:

a) from the design, selecting a candidate sub-network that includes multiple circuit elements;

b) generating a parameter based on a set of output functions performed by the selected candidate sub-network;

c) using the parameter to retrieve a replacement sub-network from a storage structure that stores replacement sub-networks; and

d) replacing the selected candidate sub-network with the replacement sub-network in the design.

3. The method of claim 2 further comprising identifying a set of output functions performed by the sub-network.

4. The method of claim 3, wherein the set of output functions includes only one output function.

5. The method of claim 3, wherein the set of output functions includes a plurality of output functions.

6. The method of claim 3, wherein each circuit element of the sub-network has an output, and each circuit element's output provides a result of one output function performed by the selected candidate sub-network.

7. The method of claim 3, wherein each circuit element of the sub-network has an output, and each output function performed by the selected candidate sub-network is provided at only a circuit-element output that fans out of the sub-network.

8. The method of claim 3, wherein a particular circuit element of the sub-network has more than one outputs, and each output of the particular circuit element provides a result of one output function performed by the selected candidate sub-network.

9. The method of claim 2 further comprising:

receiving a local function for each circuit element of the selected candidate sub-network;

identifying each output function from the received local functions.

10. The method of claim 9, wherein each local or output function is represented in terms of a binary decision diagram ("BDD"), and the sub-network has at least first and second circuit elements, wherein the first circuit element performs a first local function, and the second circuit element performs a second local function, wherein the BDD of a first output function is derived from the BDD of the first local function, and the BDD of a second output function is derived from the BDD's of at least the first and second local functions.

11. The method of claim 2 further comprising

receiving the design, wherein the design is a combinational-logic network;

selecting additional candidate sub-networks;

replacing at least some of selected additional sub-networks with replacement sub-networks retrieved from the storage structure;

wherein the replacement of the candidate sub-networks optimizes the combinational-logic network design.

12. The method of claim 2 further comprising

receiving a logical representation of the design;

converting the logical representation of the design to a circuit-level representation;

wherein selecting the candidate sub-network includes selecting the candidate sub-network from the circuit-level representation.

13. The method of claim 2, wherein the parameter is an index for storing the sub-network in the storage structure.

14. The method of claim 13, wherein the index is a numerical index.

15. The method of claim 2, wherein the parameter is a set of indices for storing the sub-network in the storage structure.

16. The method of claim 13, wherein the set of indices includes an index for each function in the set of output functions.

17. The method of claim 16, wherein the indices are numerical indices.

18. The method of claim 2 further comprising:

a) before replacing the candidate sub-network with the replacement sub-network, evaluating whether to replace the selected candidate sub-network with the replacement sub-network;

wherein said replacing is based on the evaluation.

19. The method of claim 18, wherein the evaluating comprises computing a cost function.

20. The method of claim 18 further comprising:

selecting additional candidate sub-networks;

for each candidate sub-network:

identifying at least one replacement sub-network for each selected candidate sub-network;

evaluating each identified replacement;

based on the evaluations, determining whether to replace the candidate sub-network with the replacement sub-network identified for the candidate sub-networks.

21. The method of claim 18,

wherein retrieving the replacement sub-network comprises retrieving several replacement sub-networks, the method further comprising:

evaluating each retrieved sub-network to identify viable replacement candidates;

wherein the replacement sub-network that replaces the candidate sub-network is one of the viable replacement candidates.

22. A computer readable medium storing a computer program for producing a circuit description of a design, the program comprising:

a) a first set of instruction for selecting, from the design, a candidate sub-network;

b) a second set of instruction for identifying a set of output functions performed by the sub-network;

c) a third set of instruction for retrieving, based on the identified set of output

functions, a replacement sub-network from a storage structure that stores replacement sub-networks;

d) a fourth set of instruction for replacing the selected candidate sub-network with the replacement sub-network in the design.

23. The computer readable medium of claim 22, wherein the set of output functions includes only one output function.

24. The computer readable medium of claim 22, wherein the set of output functions includes a plurality of output functions.

25. The computer readable medium of claim 22, wherein the candidate sub-network includes multiple circuit elements.